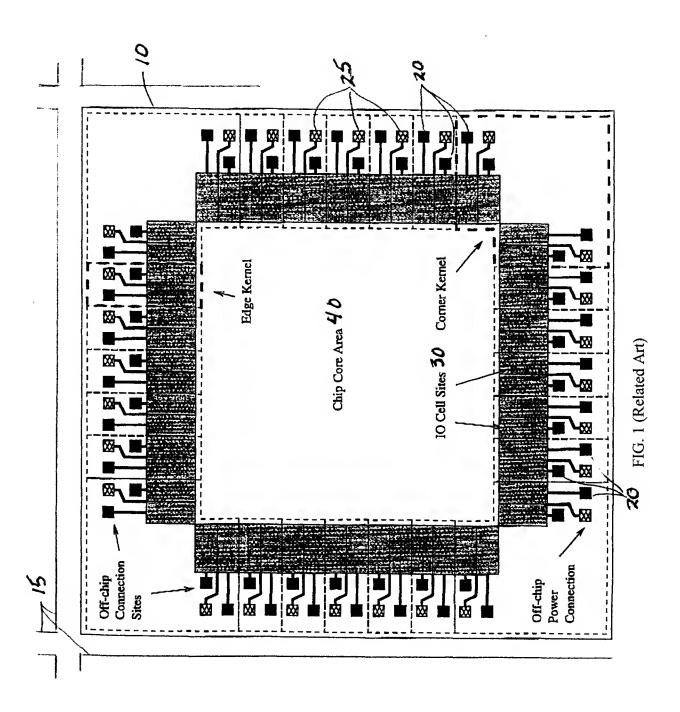
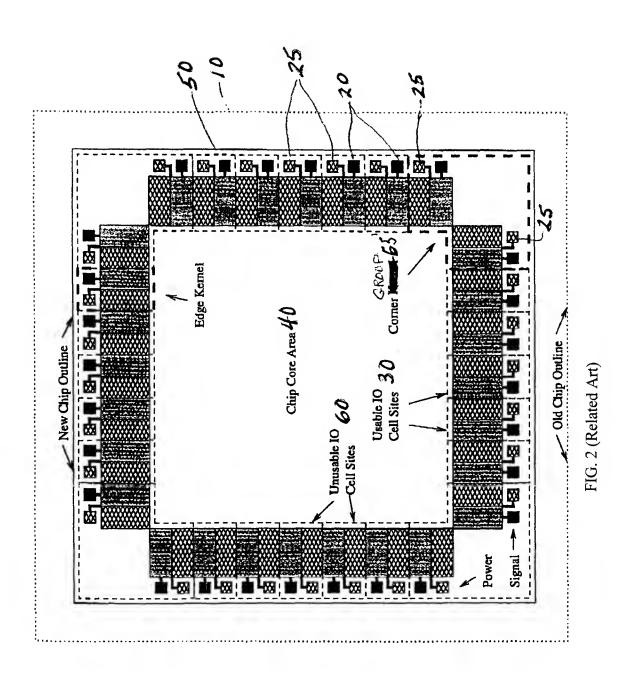
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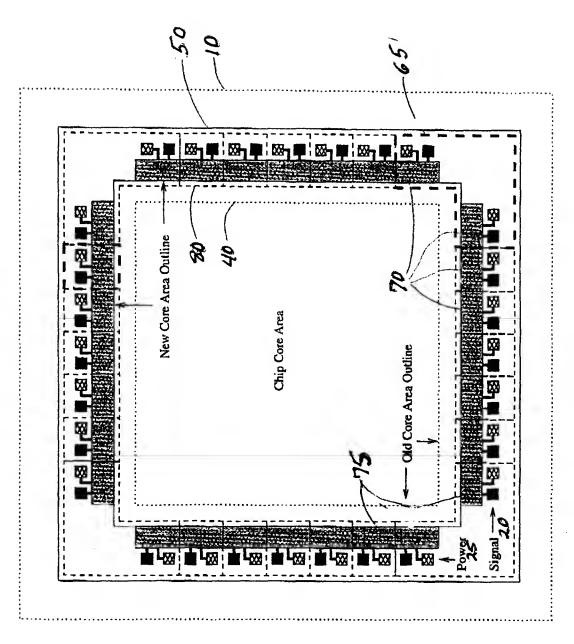
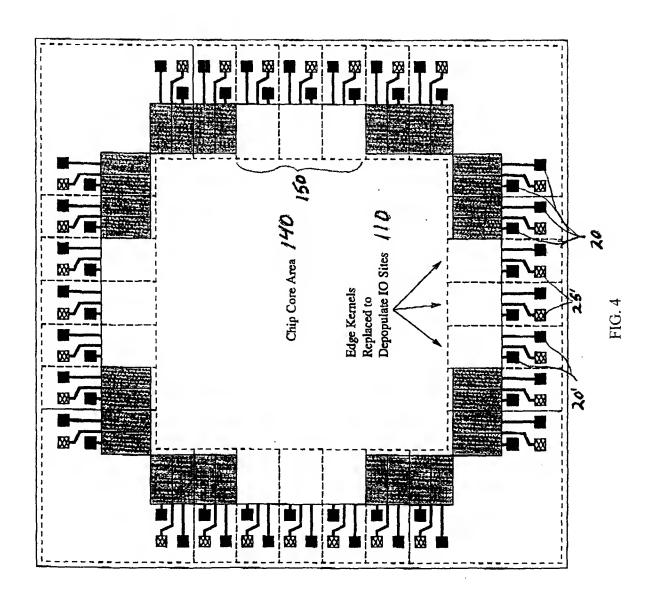
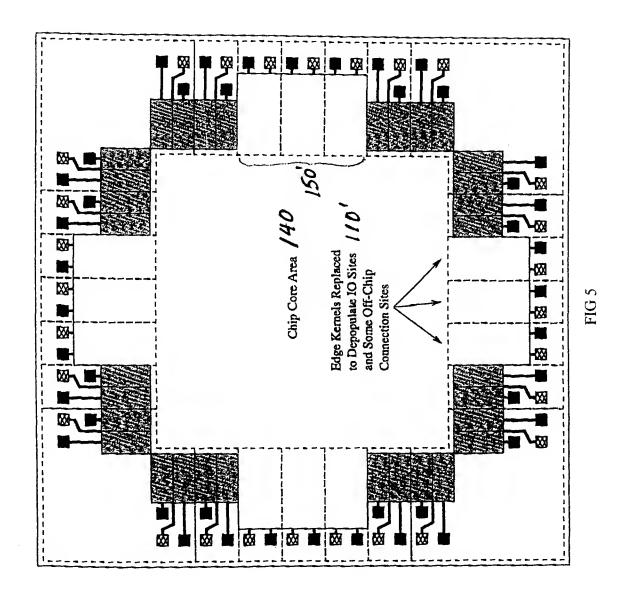


FIG. 3 (Related Art)

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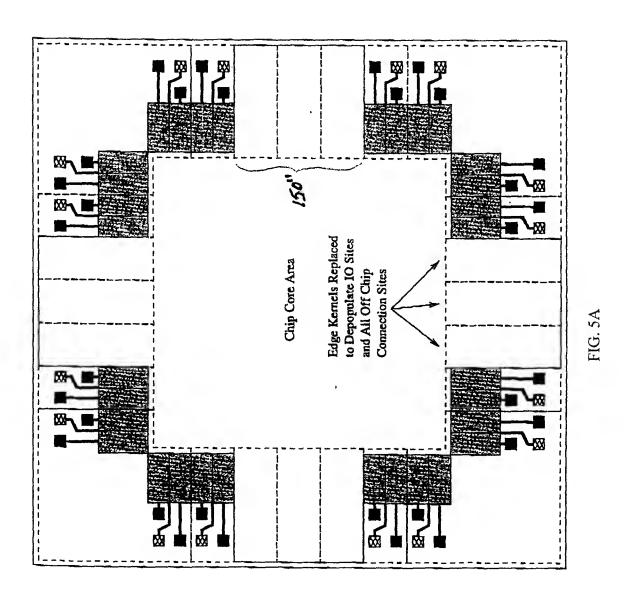


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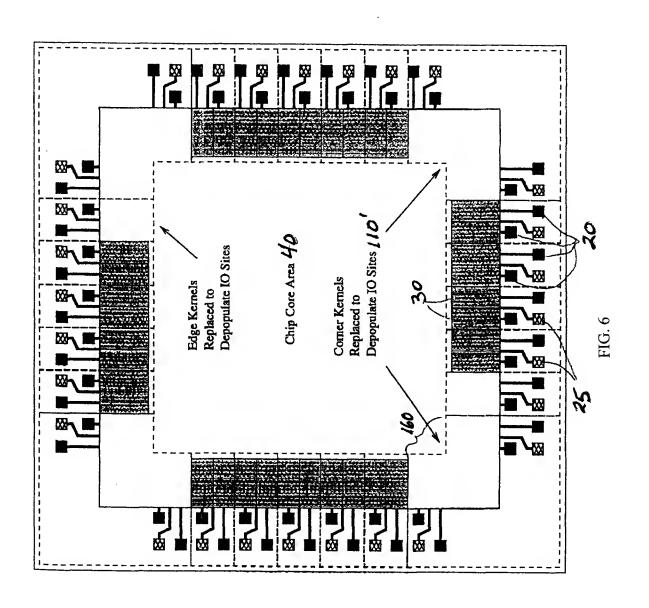


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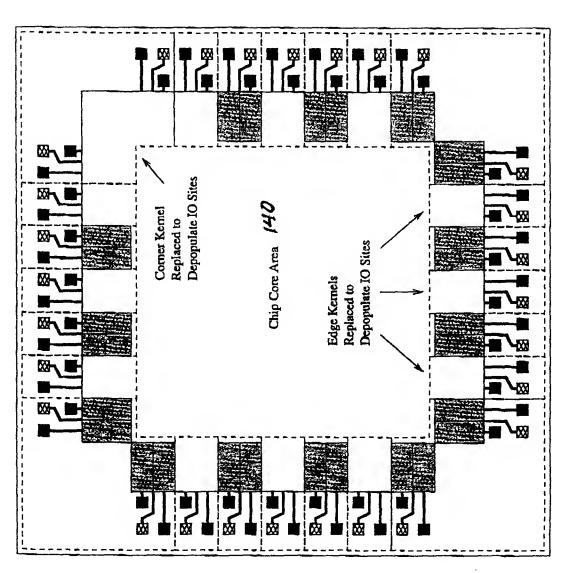


FIG. 7

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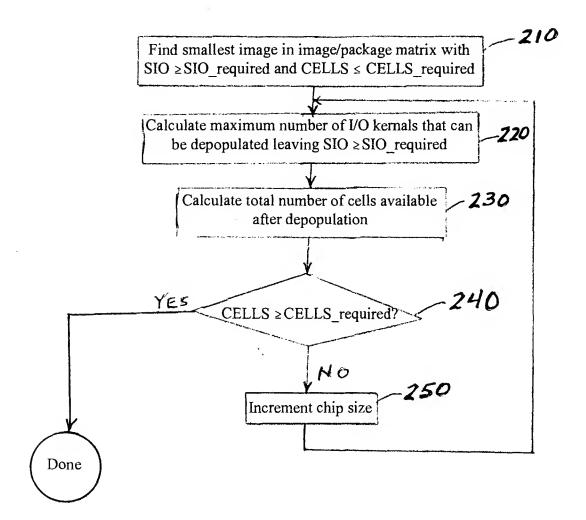
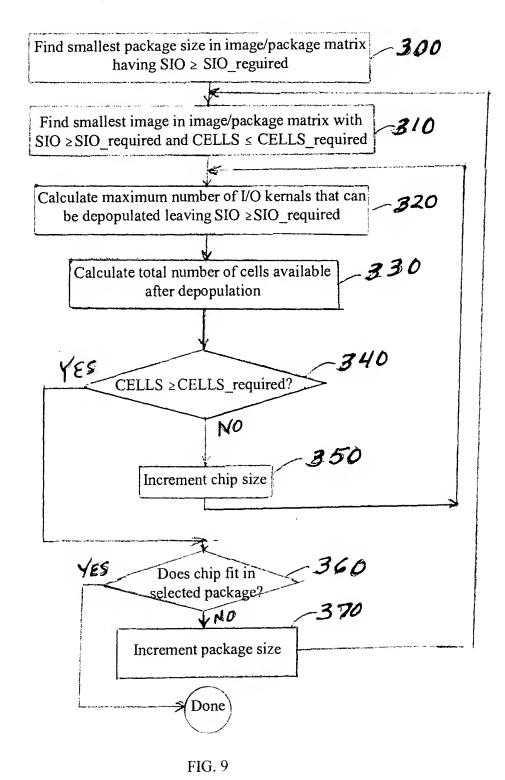


FIG. 8

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Chip Image	4.85 mm x 4.85 mm	5.58 mm x 5.58 mm	6.30 mm x 6.30 mm
Core Cell Area (dimensions)	3.89 mm x 3.89 mm	4.62 mm x 4.62 mm	5.34 mm x 5.34 mm
Core Cell Area	15.13 mm²	21.34 mm ²	28.52 mm²
Total Usable IO cell sites	352	416	480
# of adge kernel (per side)B	10	12
# of comer kernel (per comer)	1	1	

Usable IO Sites per Edge Kernel	8
Core Area Recovered by replacing an edge kernel	0.36 mm²
Usable IO Sites per Corner Kernel	24
Core Area Recovered by replacing a corner kernel	1.0 mm²

FIG. 10